AMENDMENTS TO THE ABSTRACT:

Please delete the abstract and insert the following substitute abstract after the claims.

Abstract

A data processing apparatus comprises a processor for executing a stream of instructions, and a prefetch unit for prefetching instructions from a memory prior to sending those instructions to the processor for execution. The prefetch unit receives from the memory a plurality of prefetched instructions from sequential addresses in memory, and detects whether any prefetched instructions are an instruction flow changing instruction, and outputs a fetch address for a next instruction to be prefetched by the prefetch unit. Address generation logic is also provided which, for a selected prefetched instruction that is detected to be an instruction flow changing instruction, determines a target address to be output as the fetch address. Address generation logic has a first address generation path and a further generation path for determining the target address. The first address generation path generates the target address more quickly than the further address generation path.